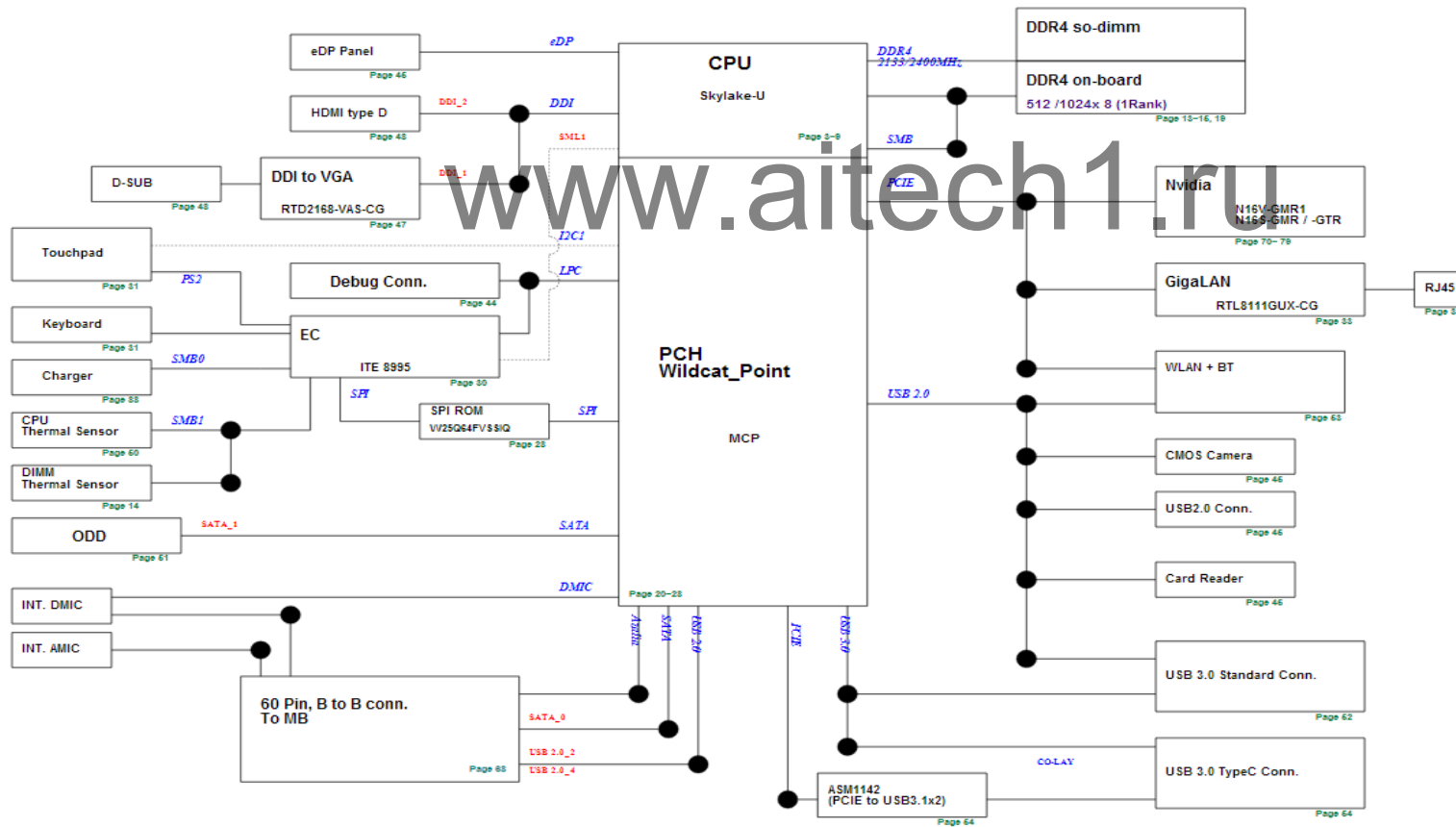


# X556 SCHEMATIC Revision 1.0

### BLOCK DIAGRAM

(UAM:UMA)  
(UV: DGPU = Nvidia N16V-GMR1)  
(UR: DGPU = Nvidia N16S-GMR)  
(UQ: DGPU = Nvidia N16S-GTR)

## Non Connected Standby



## Power

- +VCCGT
- +VCCCORE
- +VCCSA

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+1.0VSUS / +1.8VSUS

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+VCCPRIM\_CORE

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+1.35V / +0.675VS

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+3VADSW/+5VSUS

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### Load Switch

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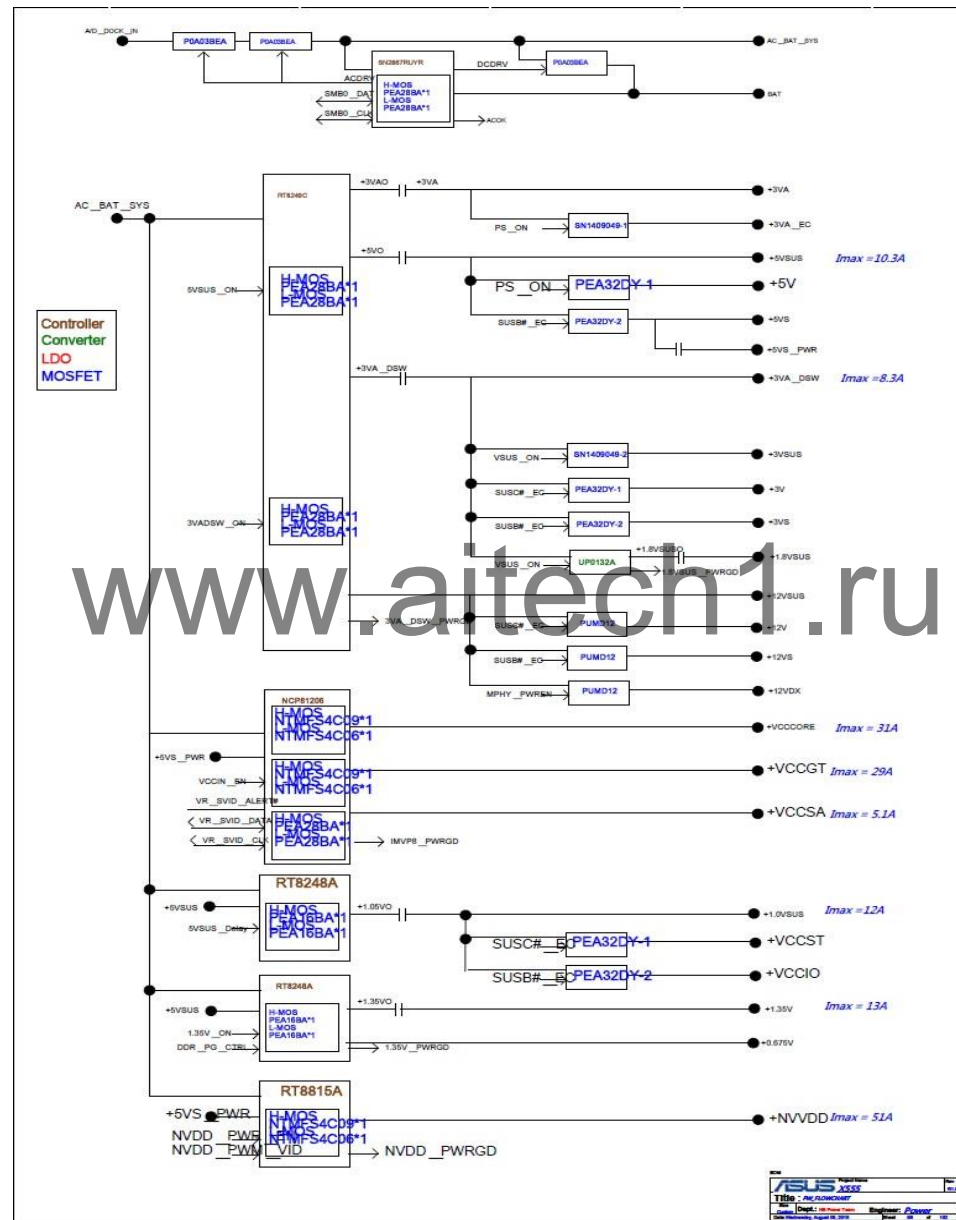
Charger

Page 8

+NVVDD

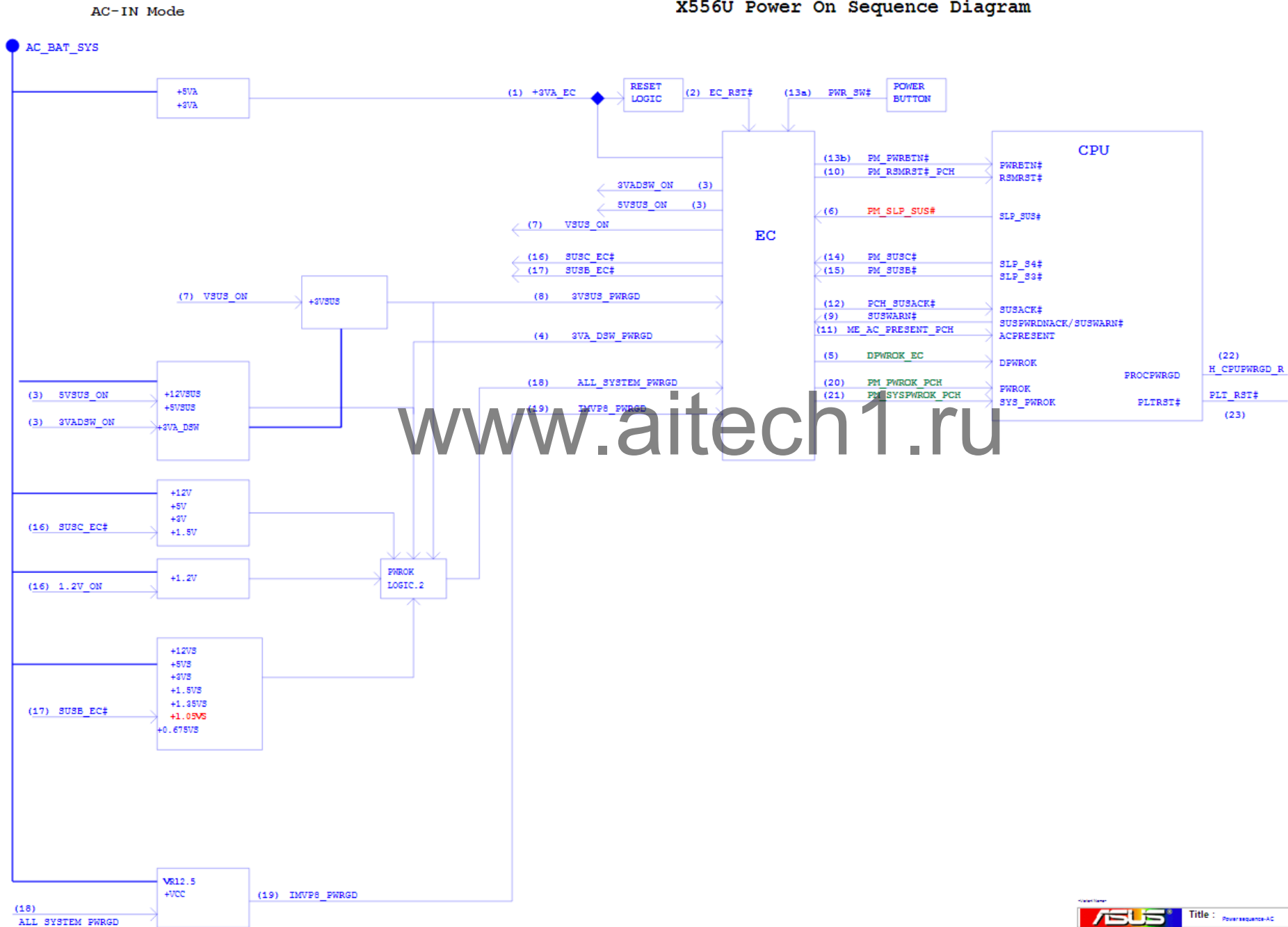
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# POWER FLOW



# POWER ON SEQUENCE

X556U Power On Sequence Diagram

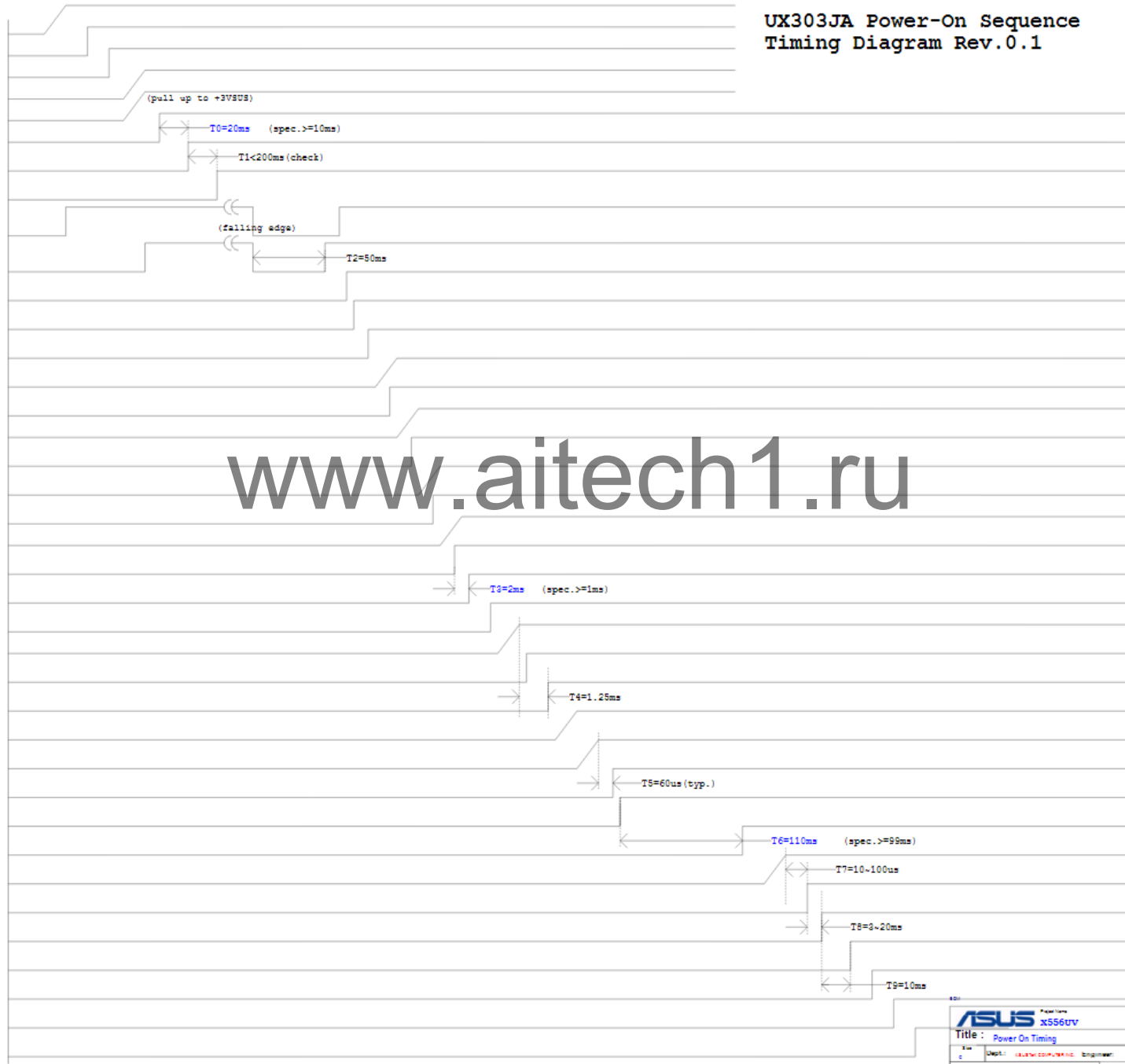


# AC POWER ON SEQUENCE

## AC-IN Mode

1 +3VA/+5VA/+3VA\_EC  
(to EC) 2 EC\_RST#  
(EC to power) 3 VSUS\_ON  
+3VSUS/+5VSUS  
(PCH to EC) 4 ME\_SusPwrDnAck  
(power to EC) 5 SUS\_PWRGD  
(EC to PCH) 6 PM\_RSMRST#  
(EC to PCH) 7 AC\_PRESENT  
(to EC) 8 PWR\_SW#  
(EC to PCH) 9 PM\_FWRBIN#  
(PCH to EC) 10 PM\_SLP\_A#  
(PCH to EC) 11 PM\_SUSC#  
12 PM\_SUSB#/SLP\_LAN#  
(PCH to EC) (PCH to power)  
+1.1VM\_LAN  
(EC to power) ME\_SLP\_M\_EC#  
+1.1VM/+3VM  
(EC to power) 13 SUSC\_EC#  
+0.6V/+1.2V/+1.8V/+3V/+5V  
(EC to power) 14 SUBS\_EC#  
+1.05V/+1.2V/+1.8V/+3V/+5V  
(power to EC) ME\_+VM\_PWRGD  
(EC to PCH) ME\_PWROK  
15 SYSTEM\_PWRGD  
+VTT\_CPU  
(CPU to power) GFX\_VR\_ON  
16 +VTT\_CPU\_PWRGD/ 17 H\_VTTPWRGD  
(power to CPU) GFX\_VID  
+VGFX\_CORE  
(power to EC) GFX\_PWRGD  
18 ALL\_SYSTEM\_PWRGD  
(EC to power) CPU\_VRON  
19 +VCCIN  
CLK\_PWRGD  
(inversion of CLK\_EN#)  
(power to EC) 20 CORE\_PWRGD  
(EC to PCH) 21 PM\_PWROK  
(PCH to CPU) H\_DRAM\_PWRGD  
(PCH to CPU) H\_CPUPWRGD  
(PCH to CPU) 22 BUF\_FLT\_RST#

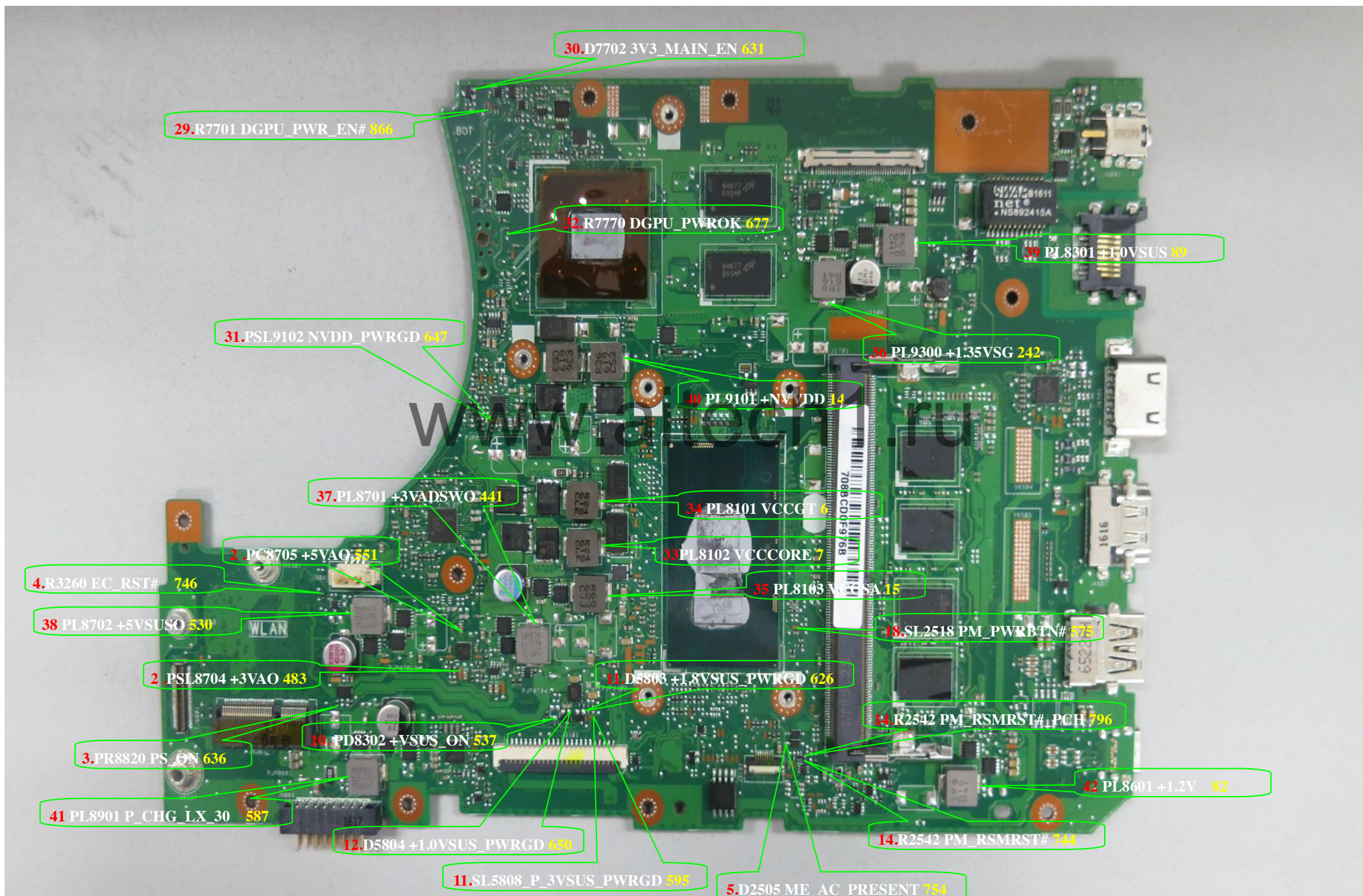
## UX303JA Power-On Sequence Timing Diagram Rev.0.1



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## Signal Measure Point-Bottom





## Signal Measure Point-Top

